

Application Note

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MPC8240 and MPC8245:
Comparison and Compatibility



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This document compares functional and hardware aspects of the MPC8240 with that of the MPC8245. It covers the following topics:

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1.1 Overview

The MPC8240 is a cost-effective, general-purpose integrated PCI bridge/memory controller processor for applications in networking infrastructure, telecommunications, and other embedded markets. It can be used for control processing in applications such as network routers and switches, mass storage subsystems, network appliances, and print and imaging systems. The MPC8245 is the second generation of the MPC8240. Like the MPC8240, it combines a G2 core microprocessor with a PCI bridge.

Both processors are comprised of a peripheral logic block and a 32-bit superscalar G2 processor core. The core can operate at a variety of frequencies, allowing the designer to trade performance for lower power consumption. The processor core is clocked from a separate PLL, which is referenced to the peripheral logic PLL. This allows the microprocessor and the peripheral logic block to operate at different frequencies while maintaining a synchronous bus interface. The interface uses a 64- or 32-bit data bus (depending on memory data bus width) and a 32-bit address bus along with control signals that enable the interface between the processor and peripheral logic to be optimized for performance.

Figure 1 shows the MPC8240 block diagram.

The features that differentiate the MPC8245 from the MPC8240 occur in the peripheral logic block. Therefore, a block diagram for the MPC8245 would include the processor core block from Figure 1 and the peripheral logic block shown in Figure 2.

Overview

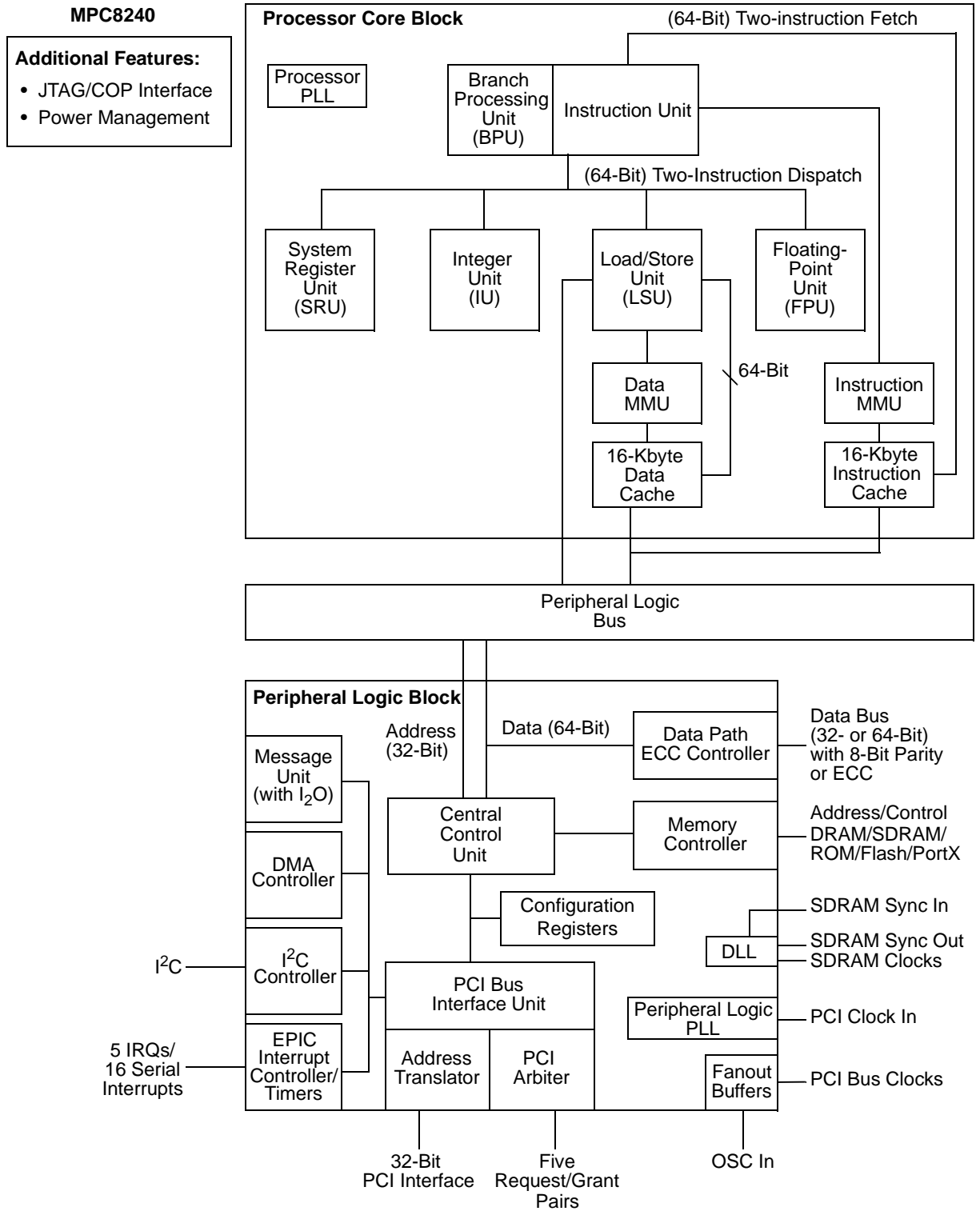


Figure 1. MPC8240 Block Diagram

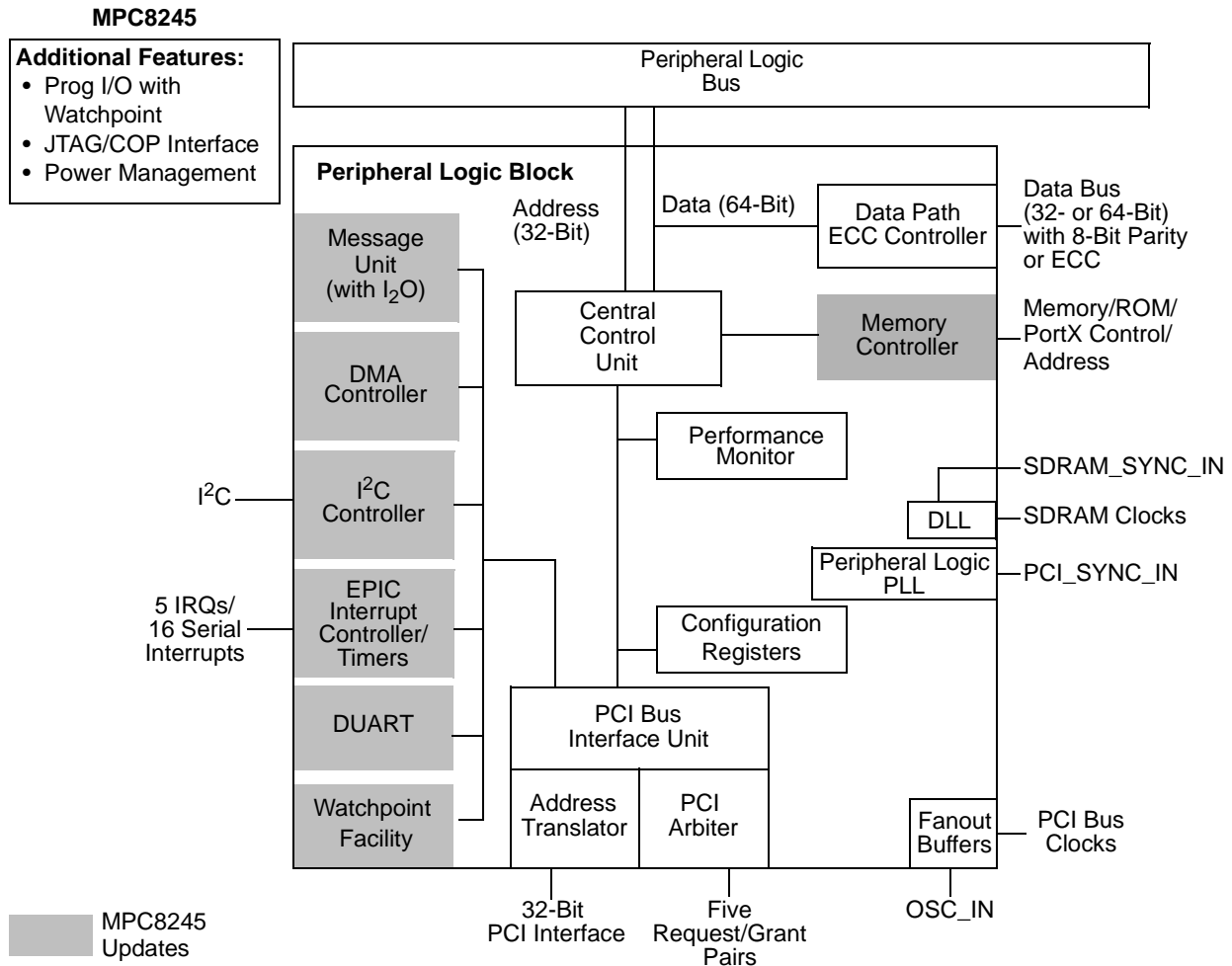


Figure 2. Peripheral Logic Block of the MPC8245

1.2 Peripheral Logic Comparison

Table 1 describes the differences between the MPC8240 and the MPC8245 peripheral logic blocks.

Table 1. Peripheral Logic Block Differences

Peripheral Logic Bus	MPC8240	MPC8245
Integrated memory controller	Supports up to 100 MHz SDRAM	Supports up to 133 MHz SDRAM
	Supports 1 to 8 banks of 16-, 64-128-, 256-Mbit memory devices	Supports 1 to 8 banks of 16-, 64- 128-, 256-, 512 -Mbit memory devices
	Supports 1-Mbyte to 1-Gbyte (s)DRAM memory	Supports 1-Mbyte to 2 -Gbyte SDRAM memory
	16 Mbytes of ROM space	272 Mbytes of ROM space selectable with reset configuration pin, SDMA1 ¹
	8-, 32-, or 64-bit PortX, I/O port	8-, 16 -, 32-, or 64-bit PortX, I/O port
	2-ROM chip selects: #0—RCS0, #1—RCS1	4 -ROM chip selects: #0—RCS0, #1—RCS1, #2—RCS2, #3—RCS3
	—	Data ready signal (DRDY) ²
	—	x16 device ³
32-bit PCI interface operating up to 66 MHz	PCI 2.1-compliant	PCI 2.2 -compliant
	—	Dual address cycle (DAC) ⁴ support for 64-bit PCI addressing
PCI agent mode capability	1 address translation unit	2 address translation units: 2 inbound and 2 outbound
New logic	—	Dual UARTs ⁵ (serial in/serial out)
	—	Configurable for a 4-pin UART ⁶
	—	Selectable with reset configuration pin, SDMA0
Embedded programmable interrupt controller (EPIC)	4 programmable timers	4 programmable timers with cascade function ⁷
Inter-integrated circuit (I ² C) controller	Supported in master and slave mode	Supported in master and slave mode with broadcast enable ability ⁸

Table 1. Peripheral Logic Block Differences (continued)

Peripheral Logic Bus	MPC8240	MPC8245
Performance monitor	—	System-level performance monitors with interrupts and PCI arbitration monitors

- ¹ Two additional reset configuration signals on the MPC8245 are not used as reset configuration signals on the MPC8240: SDMA0 and SDMA1. The SDMA0 pin selects between the MPC8245 DUART or the MPC8240 backwards-compatible mode PCI_CLK[0:4] functionality on these multiplexed signals. The default state (logic 1) of SDMA0 selects the MPC8240 backwards-compatible mode of PCI_CLK[0:4] functionality while a logic 0 state on the SDMA0 signal selects DUART functionality. Note that if using the DUART mode, four of the five PCI clocks, PCI_CLK[0:3], are not available. The SDMA1 pin selects between the MPC8245 extended ROM functionality or the MPC8240 backwards-compatible functionality on the multiplexed signals: TBEN, CHK_STOP_IN, SRESET, TRIG_IN, and TRIG_OUT. The default state (logic 1) of SDMA1 selects the MPC8240 backwards-compatible mode functionality while a logic 0 state on the SDMA1 signal selects extended ROM functionality. Note that if using the extended ROM mode, TBEN, CHK_STOP_IN, SRESET, TRIG_IN, and TRIG_OUT functionality are not available.
- ² $\overline{\text{DRDY}}$. Data ready strobe from external PortX device. It is usually asserted by an external device to indicate that a requested transaction is completed.
- ³ x16 device—PortX. A 16-bit general purpose I/O port using ROM controller interface available on $\overline{\text{RCS2}}$ and $\overline{\text{RCS3}}$.
- ⁴ Dual address cycle. Supported in master mode. Dual address cycle (DAC) command (64-bit addressing on PCI bus). DAC is different from single address cycle (SAC), in that the address phase takes two PCI beats instead of one PCI to transfer (64-bit vs. 32-bit addressing). Only PCI memory command can use DAC cycle (that is, no I/O, configuration, interrupt acknowledge, or special cycle command).
- ⁵ The DUART consists of two (dual) universal asynchronous receiver/transmitters (UARTs). The UART bus is a point-to-point bus, meaning only two UART devices are attached to the bus. The main functional areas of the UART module are serial communication channel, 16-bit counter for baud rate generation, internal channel control logic, and interrupt control logic.
- ⁶ In order for the MPC8245 to use the DUART module signals, SDMA0 must be pulled low during reset. In the special 4-pin DUART mode, bus line functions SIN1, SOUT1, SIN2, and SOUT2 are used where SIN2 and CTS1 share the same pin, and SOUT2 and RTS1 share the same pin. The clear to send (CTS) and request to send (RTS) functions are disabled. CTS and RTS are on the modem status and modem control registers, respectively.
- ⁷ Unit cascade mode gives the user the ability to treat the timers as units of measurement or 64-bit timers.
- ⁸ Broadcast enable allows the MPC8245 to accept broadcast messages from I²C bus. Broadcast is enabled by setting bit 1 of the I2CC register. This bit is reserved in the MPC8240.

1.3 Hardware Differences

The hardware differences between the MPC8240 and MPC8245 are divided into the following categories, which are discussed in the following sections:

- General parameters
- Pinout differences
- Electrical and thermal characteristics
- Operating conditions and frequency

NOTE

The MPC8241 is the lower-cost version of MPC8245. It is a 357 plastic ball grid array (PBGA) package and is functionally the same as the MPC8245, except for differences in frequency, voltage offerings, pin assignments, and packaging. Please refer to the MPC8241 hardware specifications document for details on frequency and source voltage numbers.

1.3.1 General Parameters

The nominal core V_{dd} power supply decreases from 2.5 V on the MPC8240 to 1.8/2.0 V on the MPC8245. The frequency part offerings for the MPC8245 are 266, 300, 333, 350, and 400 MHz. The frequency choices for the MPC8240 are 200 MHz (LZ200) and 250 MHz (RZ250).

Table 2. General Parameters

Parameter	MPC8240	MPC8245
Technology	0.29 μ m CMOS, five-layer metal	0.25 μ m CMOS, five-layer metal
Die size	73 mm	49.2 mm
Transistor count	3.1 million	4.5 million
Logic status	Fully static	Fully static
Package	Surface-mount 352 tape ball grid array (TBGA)	Surface-mount 352 tape ball grid array (TBGA)
Core power supply	LZU200: 100 MHz-Mem, 200 MHz-CPU, 2.5 \pm 5% V RZU250: 100 MHz-Mem, 250 MHz-CPU, 2.5–2.75 V	LZU266: 133 MHz-Mem, 266 MHz-CPU, 1.8/2.0 V \pm 100 mV ¹ LZU300: 100 MHz-Mem, 300 MHz-CPU, 1.8/2.0 V \pm 100 mV ¹ LZU333: 133 MHz-Mem, 333 MHz-CPU, 2.0 V \pm 100 mV ¹ LZU350: 100 MHz-Mem, 350 MHz-CPU, 2.0 V \pm 100 mV ¹ RZU400: 133 MHz-Mem, 400 MHz-CPU, 2.1 V \pm 100 mV ²
I/O power supply	3.0 to 3.6 V DC	3.0 to 3.6 V DC

¹ Extended temperature parts (-40° to 105°C) are available for the 266, 300, 333, and 350 MHz parts. See the part number specifications document for these parts in MPC8245TZUPNS/D.

² See the part number specifications document for this part in MPC8245RZUPNS/D.

Voltage sequencing requirements for the MPC8245 are similar to those for the MPC8240; however, there are two changes for the MPC8245. First, there is an additional requirement for the MPC8245 that the non-PCI input voltages (V_{IN}) must not be greater than either GV_{dd} or OV_{dd} by more than 0.6 V at all times, including during power-on reset. Second, for the MPC8245, LV_{dd} must not exceed OV_{dd} by more than 3.0 V at any time including during power-on reset. The allowable separation between LV_{dd} and OV_{dd} is 3.6 V for the MPC8240. See Table 3 for the definitions of the V_{dd}, LV_{dd}, OV_{dd}, and GV_{dd} as they pertain to the MPC8240 and the MPC8245.

1.3.2 Pinout Differences

Most pins in the MPC8240 and the MPC8245 have the same name and functions. However, Table 3 lists the pins that have different names and functions between the two microprocessors. For a full pin signal description, please see the appropriate hardware specifications document.

Table 3. Pinout Differences

Signal		Package Pin Number	Pin Type	Power Supply	Notes
MPC8240	MPC8245				
TRIG_IN	TRIG_IN/ $\overline{\text{RCS2}}$	AF20	Input—MPC8240 I/O—MPC8245	OVdd	1, 2
TRIG_OUT	TRIG_OUT/ $\overline{\text{RCS3}}$	AC18	I/O—MPC824 Output—MPC8245	OVdd—MPC8240 GVdd—MPC8245	1, 2
$\overline{\text{SRESET}}$	$\overline{\text{SRESET}}$ /SDMA12	B16	Input—MPC8240 I/O—MPC8245	OVdd—MPC8240 GVdd—MPC8245	1, 3
SDBA1/SDMA12	SDBA1	P1	Output	GVdd	3, 4
$\overline{\text{TEST1}}$	$\overline{\text{DRDY}}$	B20	Input	OVdd	1, 5
TBEN	TBEN/SDMA13	B14	Input—MPC8240 I/O—MPC8245	OVdd	1, 6
CHKSTOP_IN	CHKSTOP_IN/SDMA14	D14	Input—MPC8240 I/O—MPC8245	GVdd	1, 6
$\overline{\text{TEST2}}$	RTC	Y2	Input	GVdd	7
LAVdd	No Connect	D17	Power for DLL 2.5 V— MPC8240 No connection— MPC8245	LAVdd	
DUART Control/Clock Out Signals					
PCI_CLK0	PCI_CLK0/SOUT1	AC25	Output	GVdd	8
PCI_CLK1	PCI_CLK1/SIN1	AB25	I/O	GVdd	9
PCI_CLK2	PCI_CLK2/ $\overline{\text{RTS1}}$ / SOUT2	AE26	Output	GVdd	8
PCI_CLK3	PCI_CLK3/ $\overline{\text{CTS1}}$ / SIN2	AF25	I/O	GVdd	9

¹ Recommend a weak pull-up resistor (2 k Ω –10 k Ω) be placed on this OVdd pin.

² The pins TRIG_IN and TRIG_OUT have the optional function of $\overline{\text{RCS2}}$ and $\overline{\text{RCS3}}$. These are additional ROM bank selects.

³ SDMA12 was switched from the option of sharing with the SDBA1 pin on the MPC8240, to sharing on the $\overline{\text{SRESET}}$ pin of the MPC8245.

⁴ Non-DRAM access output valid specification applies to this pin during non-DRAM accesses.

⁵ New signal function, $\overline{\text{DRDY}}$ —data ready strobe from PortX device.

⁶ New signal is one of two new address bits for the most significant address bits (SDMA14, SDMA13) on the MPC8245.

⁷ Recommend a weak pull-up resistor (2 k Ω –10 k Ω) be placed on this pin to GVdd.

⁸ Serial output (SOUT) data and request to send (RTS) signals for UART transactions.

⁹ Serial in (SIN) and clear to send (CTS) signals representing data received on the UART receiver serial data input signal, with the least-significant bit received first.

1.3.2.1 DUART

The DUART consists of two universal asynchronous receiver/transmitters (UARTs). The UARTs act independently and each module interfaces with the CPU. The modules are also accessible from the PCI bus.

Hardware Differences

The UART bus module consists of the following major functional areas: serial communication channel, 16-bit counter for baud rate generation, internal channel control logic, and interrupt control logic. The DUART communication channel provides a full-duplex asynchronous receiver that operates on frequency from the local memory clock.

The transmitter accepts parallel data from the CPU or PCI bus with a write to the transmitter holding register. This data is converted to serial data by the internal transmitter shift register. The receiver accepts the serial data and reconverts it to parallel format and transfers the assembled character from the receiver buffer to the processor or PCI bus in response to a read of the UART receiver buffer register. The receiver status may be polled or interrupt-driven.

1.3.3 Electrical and Thermal Characteristics

1.3.3.1 Absolute Maximum Ratings

Table 4 lists the absolute maximum rating differences between the two components.

Table 4. Absolute Maximum Rating Differences

Characteristic ¹	Symbol	MPC8240	MPC8245	Unit
Supply Voltage—CPU Core and Peripheral Logic	Vdd	−0.3 to 2.75	−0.3 to 2.1	V
Supply Voltage—Memory Bus Drivers	GVdd	−0.3 to 3.6	−0.3 to 3.6	V
Supply Voltage—PCI and Standard I/O Buffers	OVdd	−0.3 to 3.6	−0.3 to 3.6	V
Supply Voltage—PLLs	AVdd/AVdd2/LAVdd	−0.3 to 2.75	—	V
	AVdd/AVdd2	—	−0.3 to 2.1	V
Supply Voltage—PCI Reference	LVdd	−0.3 to 5.4	−0.3 to 5.4	V
Input Voltage ²	V _{IN}	−0.3 to 3.6	−0.3 to 3.6	V
Operational Die-Junction Temperature Range	T _J	0 to 105	0 to 105 ³	°C
Storage Temperature Range	T _{STG}	−55 to 150	−55 to 150	°C

¹ Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

² PCI inputs with LVdd = 5 V ± 5% V DC may be correspondingly stressed at voltages exceeding LVdd + 0.5 V DC.

³ See part number specifications documents for XPC8245RZUxxxPNS and XPC8245TZUxxxPNS.

1.3.3.2 Recommended Operating Conditions

For the most part, the operating conditions between the MPC8245 and the MPC8240 are the same; however, under certain conditions, some differences exist. Table 5 shows conditions under which these variances occur.

Hardware Differences

Table 6. PLL Configurations for MPC8240

Ref	PLL_CFG [0:4] ¹	CPU ² HID1 [0:4]	250 MHz ³			200 MHz ³			Multipliers ^{4, 5}	
			PCI Clock Input (PCI_SYNC_IN) Range (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI to Mem (Mem VCO)	Mem to CPU (CPU VCO)
0	00000	00110	25–33	75–100	188–250	25–26	75–80	188–200	3 (6)	2.5 (5)
1	00001	11000	25–27	75–83	225–250	Not Usable			3 (6)	3 (6)
2	00010	00101	50–56 ⁶	50–56	100–112	50–56 ⁶	50–56	100–112	1 (4)	2 (8)
3	00011	00101	Bypass			Bypass			Bypass	2 (8)
4	00100	00101	25–28 ⁶	50–56	100–113	25–28 ⁶	50–56	100–113	2 (8)	2 (8)
5	00101	00110	Bypass			Bypass			Bypass	2.5 (5)
7	00111	11000	Bypass			Bypass			Bypass	3 (6)
8	01000	11000	33 ⁷ –56 ⁶	33–56	100–168	33 ⁷ –56 ⁶	33–56	100–168	1 (4)	3 (6)
A	01010	00111	25–27	50–55	225–250	Not Usable			2 (4)	4.5 (9)
C	01100	00110	25–50	50–100	125–250	25–40	50–80	125–200	2 (4)	2.5 (5)
E	01110	11000	25–41	50–83	150–250	25–33	50–66	150–200	2 (4)	3 (6)
10	10000	00100	25–33	75–100	150–200	25–33	75–100	150–200	3 (6)	2 (4)
12	10010	00100	33–66	50–100	100–200	33 ⁸ –66	50–100	100–200	1.5 (3)	2 (4)
14	10100	11110	25–35	50–71	175–250	25–28	50–56	175–200	2 (4)	3.5 (7)
16	10110	11010	25–31	50–62	200–250	25	50	200	2 (4)	4 (8)
18	11000	11000	25–33	62–83	186–250	25–26	62–65	186–200	2.5 (5)	3 (6)
1A	11010	11010	50 ⁸ –62	50–62	200–250	50	50	200	1 (2)	4 (8)
1C	11100	11000	33 ⁸ –55	50–83	150–250	33 ⁸ –44	50–66	150–200	1.5 (3)	3 (6)
1D	11101	00110	33 ⁸ –66	50–100	125–250	33 ⁸ –53	50–80	125–200	1.5 (3)	2.5 (5)
1E	11110	01111	Not Usable						Off	Off
1F	11111	11111	Not Usable						Off	Off

¹ PLL_CFG[0:4] settings not listed (00110, 01001, 01011, 01101, 01111, 10001, 10011, 10101, 10111, 11001, and 11011) are reserved.

² The processor HID1 values only represent the multiplier of the processor's PLL (memory to processor multiplier). Thus, multiple MPC8240 PLL_CFG[0:4] values may have the same processor HID1 value. This implies that system software cannot read the HID1 register and associate it with a unique PLL_CFG[0:4] value.

³ Range values are shown rounded down to the nearest whole number (decimal place accuracy removed) for clarity.

⁴ In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for factory use only. The AC timing specifications given in this document do not apply in PLL bypass mode.

⁵ In clock off mode, no clocking occurs inside the MPC8240 regardless of the PCI_SYNC_IN input.

⁶ Limited due to maximum memory VCO = 225 MHz.

⁷ Limited due to minimum CPU VCO = 200 MHz.

⁸ Limited due to minimum memory VCO = 100 MHz.

The MPC8245 PLL_CFG[0:4] setting 0x02 (0b00010) has a different PCI-to-Mem and Mem-to-CPU multiplier ratio than the same setting on the MPC8240, and thus, is not backwards-compatible.

Some PLL configurations may not be fully backwards-compatible between the MPC8240 and the MPC8245. For example, the MPC8245 PLL_CFG[0:4] setting 0x0C (0b01100) is capable of accepting a subset of the PCI_SYNC_IN input frequency range of that of the MPC8240, and thus, may not be fully backwards-compatible. Also note that certain PLL configurations available in the MPC8245 are not available in the MPC8240. For example, configuration 0x11 (0b10001) does not exist on the MPC8240, but is available in the MPC8245. Table 7 through Table 9 show the PLL settings for the MPC8245. Note that five CPU frequency offerings are available: 266 MHz, 300 MHz, 333 MHz, 350 MHz, and 400 MHz.

Table 7. PLL Configurations (266- and 300-MHz Parts)

Ref	PLL_CFG [0:4] ^{10,13}	266 MHz Part ⁹			300 MHz Part ⁹			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range ¹ (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range ¹ (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI to Mem (Mem VCO)	Mem to CPU (CPU VCO)
0	00000 ¹²	25 - 35 ⁵	75 - 105	188 - 263	25 - 40 ⁵	75 - 120	188 - 300	3 (2)	2.5 (2)
1	00001 ¹²	25 - 29 ⁵	75 - 88	225 - 264	25 - 33 ⁵	75 - 99	225 - 297	3 (2)	3 (2)
2	00010 ¹¹	50 ¹⁸ - 59 ⁵	50 - 59	225 - 266	50 ¹⁸ - 66 ¹	50 - 66	225 - 297	1 (4)	4.5 (2)
3	00011 ^{11,14}	50 ⁴ - 66 ¹	50 - 66	100 - 133	50 ⁴ - 66 ¹	50 - 66	100 - 133	1 (Bypass)	2 (4)
4	00100 ¹²	25 - 46 ⁴	50 - 92	100 - 184	25 - 46 ⁴	50 - 92	100 - 184	2 (4)	2 (4)
5	00101	Reserved			Reserved			Note 20	
6	00110 ¹⁵	Bypass			Bypass			Bypass	
7	00111 ¹⁴	60 ⁶ - 66 ¹	60 - 66	180 - 198	60 ⁶ - 66 ¹	60 - 66	180 - 198	1 (Bypass)	3 (2)
8	01000 ¹²	60 ⁶ - 66 ¹	60 - 66	180 - 198	60 ⁶ - 66 ¹	60 - 66	180 - 198	1 (4)	3 (2)
9	01001 ¹⁹	45 ⁶ - 66 ¹	90 - 132	180 - 264	45 ⁶ - 66 ¹	90 - 132	180 - 264	2 (2)	2 (2)
A	01010 ¹²	25 - 29 ⁵	50 - 58	225 - 261	25 - 33 ⁵	50 - 66	225 - 297	2 (4)	4.5 (2)
B	01011 ¹⁹	45 ³ - 59 ⁵	68 - 88	204 - 264	45 ³ - 66 ¹	68 - 99	204 - 297	1.5 (2)	3 (2)
C	01100 ¹²	36 ⁶ - 46 ⁴	72 - 92	180 - 230	36 ⁶ - 46 ⁴	72 - 92	180 - 230	2 (4)	2.5 (2)
D	01101 ¹⁹	45 ³ - 50 ⁵	68 - 75	238 - 263	45 ³ - 57 ⁵	68 - 85	238 - 298	1.5 (2)	3.5 (2)
E	01110 ¹²	30 ⁶ - 44 ⁵	60 - 88	180 - 264	30 ⁶ - 46 ⁴	60 - 92	180 - 276	2 (4)	3 (2)
F	01111 ¹⁹	25 ⁵	75	263	25 - 28 ⁵	75 - 85	263 - 298	3 (2)	3.5 (2)
10	10000 ¹²	30 ⁶ - 44 ^{2,5}	60 - 132	180 - 264	30 ⁶ - 44 ²	60 - 132	180 - 264	3 (2)	2 (2)
11	10001 ¹⁹	25 - 26 ⁵	100 - 106	250 - 266	25 - 29 ²	100 - 116	250 - 290	4 (2)	2.5 (2)
12	10010 ¹²	60 ⁶ - 66 ¹	90 - 99	180 - 198	60 ⁶ - 66 ¹	90 - 99	180 - 198	1.5 (2)	2 (2)
13	10011 ¹⁹	Not Available			25 ²	100	300	4 (2)	3 (2)
14	10100 ¹²	26 ⁶ - 38 ⁵	52 - 76	182 - 266	26 ⁶ - 42 ⁵	52 - 84	182 - 294	2 (4)	3.5 (2)
15	10101 ¹⁹	Not Available			27 ³ - 30 ⁵	68 - 75	272 - 300	2.5 (2)	4 (2)
16	10110 ¹²	25 - 33 ⁵	50 - 66	200 - 264	25 - 37 ⁵	50 - 74	200 - 296	2 (4)	4 (2)

Hardware Differences

Table 7. PLL Configurations (266- and 300-MHz Parts) (continued)

Ref	PLL_CFG [0:4] ^{10,13}	266 MHz Part ⁹			300 MHz Part ⁹			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range ¹ (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range ¹ (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI to Mem (Mem VCO)	Mem to CPU (CPU VCO)
17	10111 ¹⁹	25 - 33 ⁵	100 - 132	200 - 264	25 - 33 ²	100 - 132	200 - 264	4 (2)	2 (2)
18	11000 ¹²	27 ³ - 35 ⁵	68 - 88	204 - 264	27 ³ - 40 ⁵	68 - 100	204 - 300	2.5 (2)	3 (2)
19	11001 ¹⁹	36 ⁶ - 53 ⁵	72 - 106	180 - 265	36 ⁶ - 59 ²	72 - 118	180 - 295	2 (2)	2.5 (2)
1A	11010 ¹²	50 ¹⁸ - 66 ¹	50 - 66	200 - 264	50 ¹⁸ - 66 ¹	50 - 66	200 - 264	1 (4)	4 (2)
1B	11011 ¹⁹	33 ⁶ - 44 ⁵	66 - 88	198 - 264	33 ⁶ - 50 ⁵	66 - 100	198 - 300	2 (2)	3 (2)
1C	11100 ¹²	44 ⁶ - 59 ⁵	66 - 88	198 - 264	44 ⁶ - 66 ¹	66 - 99	198 - 297	1.5 (2)	3 (2)
1D	11101 ¹²	48 ⁶ - 66 ¹	72 - 99	180 - 248	48 ⁶ - 66 ¹	72 - 99	180 - 248	1.5 (2)	2.5 (2)
1E	11110 ⁸	Not Usable			Not Usable			Off	Off
1F	11111 ⁸	Not Usable			Not Usable			Off	Off

¹ Limited by maximum PCI input frequency (66 MHz).

² Limited by maximum system memory interface operating frequency (100 MHz @ 350 MHz CPU).

³ Limited by minimum memory VCO frequency (133 MHz).

⁴ Limited due to maximum memory VCO frequency (372 MHz).

⁵ Limited by maximum CPU operating frequency (266 MHz).

⁶ Limited by minimum CPU VCO frequency (360 MHz).

⁷ Limited by maximum CPU VCO frequency (800 MHz).

⁸ In clock off mode, no clocking occurs inside the MPC8245 regardless of the PCI_SYNC_IN input.

⁹ Range values are shown rounded down to the nearest whole number (decimal place accuracy removed) for clarity.

¹⁰ PLL_CFG[0:4] settings not listed (01011, 01101, 01111, 10001, 10011, 10101, 11001, and 11011) are reserved.

¹¹ Multiplier ratios for this PLL_CFG[0:4] setting are different from the MPC8240 and are not backwards-compatible.

¹² PCI_SYNC_IN range for this PLL_CFG[0:4] setting is different from the MPC8240 and may not be fully backwards-compatible.

¹³ Bits 7–4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value.

¹⁴ In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for hardware modeling support. The AC timing specifications given in this document do not apply in PLL bypass mode.

¹⁵ In dual PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation, and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is intended for hardware modeling support. The AC timing specifications given in this document do not apply in dual PLL bypass mode.

¹⁶ Limited by maximum system memory interface operating frequency (133 MHz @ 266 MHz CPU).

¹⁷ Limited by minimum CPU operating frequency (100 MHz).

¹⁸ Limited by minimum memory bus frequency (50 MHz).

¹⁹ PCI_SYNC_IN range for this PLL_CFG[0:4] setting does not exist on the MPC8240 and may not be fully backwards-compatible.

²⁰ No longer supported.

Hardware Differences

Table 8. PLL Configurations (333- and 350-MHz Parts)

Ref	PLL_CFG [0:4] ^{10,13}	333 MHz Part ⁹			350 MHz Part ⁹			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range ¹ (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range ¹ (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI to Mem (Mem VCO)	Mem to CPU (CPU VCO)
0	00000 ¹²	25 - 44 ¹⁶	75 - 132	188 - 330	25 - 44 ¹⁶	75 - 132	188 - 330	3 (2)	2.5 (2)
1	00001 ¹²	25 - 37 ⁵	75 - 111	225 - 333	25 - 38 ⁵	75 - 114	225 - 342	3 (2)	3 (2)
2	00010 ¹¹	50 ¹⁸ - 66 ¹	50 - 66	225 - 297	50 ¹⁸ - 66 ¹	50 - 66	225 - 297	1 (4)	4.5 (2)
3	00011 ^{11,14}	50 ⁴ - 66 ¹	50 - 66	100 - 133	50 ⁴ - 66 ¹	50 - 66	100 - 133	1 (Bypass)	2 (4)
4	00100 ¹²	25 - 46 ⁴	50 - 92	100 - 184	25 - 46 ⁴	50 - 92	100 - 184	2 (4)	2 (4)
5	00101	Reserved			Reserved			Note 20	
6	00110 ¹⁵	Bypass			Bypass			Bypass	
7	00111 ¹⁴	60 ⁶ - 66 ¹	60 - 66	180 - 198	60 ⁶ - 66 ¹	60 - 66	180 - 198	1 (Bypass)	3 (2)
8	01000 ¹²	60 ⁶ - 66 ¹	60 - 66	180 - 198	60 ⁶ - 66 ¹	60 - 66	180 - 198	1 (4)	3 (2)
9	01001 ¹⁹	45 ⁶ - 66 ¹	90 - 132	180 - 264	45 ⁶ - 66 ¹	90 - 132	180 - 264	2 (2)	2 (2)
A	01010 ¹²	25 - 37 ⁵	50 - 74	225 - 333	25 - 38 ⁵	50 - 76	225 - 342	2 (4)	4.5 (2)
B	01011 ¹⁹	45 ³ - 66 ¹	68 - 99	204 - 297	45 ³ - 66 ¹	68 - 99	204 - 297	1.5 (2)	3 (2)
C	01100 ¹²	36 ⁶ - 46 ⁴	72 - 92	180 - 230	36 ⁶ - 46 ⁴	72 - 92	180 - 230	2 (4)	2.5 (2)
D	01101 ¹⁹	45 ³ - 63 ⁵	68 - 95	238 - 333	45 ³ - 66 ¹	68 - 99	238 - 347	1.5 (2)	3.5 (2)
E	01110 ¹²	30 ⁶ - 46 ⁴	60 - 92	180 - 276	30 ⁶ - 46 ⁴	60 - 92	180 - 276	2 (4)	3 (2)
F	01111 ¹⁹	25 - 31 ⁵	75 - 93	263 - 326	25 - 33 ⁵	75 - 99	263 - 347	3 (2)	3.5 (2)
10	10000 ¹²	30 ⁶ - 44 ²	60 - 132	180 - 264	30 ⁶ - 44 ²	60 - 132	180 - 264	3 (2)	2 (2)
11	10001 ¹⁹	25 - 33 ²	100 - 132	250 - 330	25 - 33 ²	100 - 132	250 - 330	4 (2)	2.5 (2)
12	10010 ¹²	60 ⁶ - 66 ¹	90 - 99	180 - 198	60 ⁶ - 66 ¹	90 - 99	180 - 198	1.5 (2)	2 (2)
13	10011 ¹⁹	25 - 27 ⁵	100 - 108	300 - 324	25 - 29 ⁵	100 - 116	300 - 348	4 (2)	3 (2)
14	10100 ¹²	26 ⁶ - 47 ⁴	52 - 94	182 - 329	26 ⁶ - 47 ⁴	52 - 94	182 - 329	2 (4)	3.5 (2)
15	10101 ¹⁹	27 ³ - 33 ⁵	68 - 83	272 - 332	27 ³ - 34 ⁵	68 - 85	272 - 340	2.5 (2)	4 (2)
16	10110 ¹²	25 - 41 ⁵	50 - 82	200 - 328	25 - 43 ⁵	50 - 86	200 - 344	2 (4)	4 (2)
17	10111 ¹⁹	25 - 33 ²	100 - 132	200 - 264	25 - 33 ²	100 - 132	200 - 264	4 (2)	2 (2)
18	11000 ¹²	27 ³ - 44 ⁵	68 - 110	204 - 330	27 ³ - 46 ⁵	68 - 115	204 - 345	2.5 (2)	3 (2)
19	11001 ¹⁹	36 ⁶ - 66 ¹	72 - 132	180 - 330	36 ⁶ - 66 ¹	72 - 132	180 - 330	2 (2)	2.5 (2)
1A	11010 ¹²	50 ¹⁸ - 66 ¹	50 - 66	200 - 264	50 ¹⁸ - 66 ¹	50 - 66	200 - 264	1 (4)	4 (2)
1B	11011 ¹⁹	33 ⁶ - 55 ⁵	66 - 110	198 - 330	33 ⁶ - 58 ⁵	66 - 116	198 - 348	2 (2)	3 (2)
1C	11100 ¹²	44 ⁶ - 66 ¹	66 - 99	198 - 297	44 ⁶ - 66 ¹	66 - 99	198 - 297	1.5 (2)	3 (2)
1D	11101 ¹²	48 ⁶ - 66 ¹	72 - 99	180 - 248	48 ⁶ - 66 ¹	72 - 99	180 - 248	1.5 (2)	2.5(2)
1E	11110 ⁸	Not Usable			Not Usable			Off	Off

Table 8. PLL Configurations (333- and 350-MHz Parts) (continued)

Ref	PLL_CFG [0:4] ^{10,13}	333 MHz Part ⁹			350 MHz Part ⁹			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range ¹ (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range ¹ (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI to Mem (Mem VCO)	Mem to CPU (CPU VCO)
1F	11111 ⁸	Not Usable			Not Usable			Off	Off

- ¹ Limited by maximum PCI input frequency (66 MHz).
- ² Limited by maximum system memory interface operating frequency (100 MHz @ 350 MHz CPU).
- ³ Limited by minimum memory VCO frequency (133 MHz).
- ⁴ Limited due to maximum memory VCO frequency (372 MHz).
- ⁵ Limited by maximum CPU operating frequency (266 MHz).
- ⁶ Limited by minimum CPU VCO frequency (360 MHz).
- ⁷ Limited by maximum CPU VCO frequency (800 MHz).
- ⁸ In clock off mode, no clocking occurs inside the MPC8245 regardless of the PCI_SYNC_IN input.
- ⁹ Range values are shown rounded down to the nearest whole number (decimal place accuracy removed) for clarity.
- ¹⁰ PLL_CFG[0:4] settings not listed (01011, 01101, 01111, 10001, 10011, 10101, 11001, and 11011) are reserved.
- ¹¹ Multiplier ratios for this PLL_CFG[0:4] setting are different from the MPC8240 and are not backwards-compatible.
- ¹² PCI_SYNC_IN range for this PLL_CFG[0:4] setting is different from the MPC8240 and may not be fully backwards-compatible.
- ¹³ Bits 7–4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value.
- ¹⁴ In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for hardware modeling support. The AC timing specifications given in this document do not apply in PLL bypass mode.
- ¹⁵ In dual PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation, and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is intended for hardware modeling support. The AC timing specifications given in this document do not apply in dual PLL bypass mode.
- ¹⁶ Limited by maximum system memory interface operating frequency (133 MHz @ 333 MHz CPU).
- ¹⁷ Limited by minimum CPU operating frequency (100 MHz).
- ¹⁸ Limited by minimum memory bus frequency (50 MHz).
- ¹⁹ PCI_SYNC_IN range for this PLL_CFG[0:4] setting does not exist on the MPC8240 and may not be fully backwards-compatible.
- ²⁰ No longer supported.

Table 9. MPC8245 PLL Configurations for 400-MHz Part Offering

Ref	PLL_CFG[0:4] ^{10,13}	400 MHz Part ⁹			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range ¹ (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI to Mem (Mem VCO)	Mem to CPU (CPU VCO)
0	00000 ¹²	25 - 44 ²	75 - 132	188 - 330	3 (2)	2.5 (2)
1	00001 ¹²	25 - 44 ⁵	75 - 132	225 - 396	3 (2)	3 (2)
2	00010 ¹¹	50 ¹⁷ - 66 ¹	50 - 66	225 - 297	1 (4)	4.5 (2)
3	00011 ^{11,14}	50 ¹⁶ - 66 ¹	50 - 66	100 - 133	1(Bypass)	2 (4)
4	00100 ¹²	25 - 46 ⁴	50 - 92	100 - 184	2 (4)	2 (4)
6	00110 ¹⁵	Bypass			Bypass	Bypass
7	00111 ¹⁴	60 ⁶ - 66 ¹	60 - 66	180 - 198	1(Bypass)	3 (2)
8	01000 ¹²	60 ⁶ - 66 ¹	60 - 66	180 - 198	1 (4)	3 (2)
9	01001 ¹⁸	45 ⁶ - 66 ¹	90 - 132	180 - 264	2 (2)	2 (2)
A	01010 ¹²	25 - 44 ⁵	50 - 88	225 - 396	2 (4)	4.5 (2)
B	01011 ¹⁸	45 ³ - 66 ¹	68 - 99	204 - 297	1.5 (2)	3 (2)
C	01100 ¹²	36 ⁶ - 46 ⁴	72 - 92	180 - 230	2 (4)	2.5 (2)
D	01101 ¹⁸	45 ³ - 66 ¹	68 - 99	238 - 347	1.5 (2)	3.5 (2)
E	01110 ¹²	30 ⁶ - 46 ⁴	60 - 92	180 - 276	2 (4)	3 (2)
F	01111 ¹⁸	25 - 38 ⁵	75 - 114	263 - 399	3(2)	3.5(2)
10	10000 ¹²	30 ⁶ - 44 ²	60 - 132	180 - 264	3 (2)	2 (2)
11	10001 ¹⁸	25 - 33 ²	100 - 132	250 - 330	4(2)	2.5(2)
12	10010 ¹²	60 ⁶ - 66 ¹	90 - 99	180 - 198	1.5 (2)	2 (2)
13	10011 ¹⁸	25 - 33 ⁵	100 - 132	300 - 396	4(2)	3(2)
14	10100 ¹²	26 ⁶ - 47 ⁴	52 - 94	182 - 329	2 (4)	3.5 (2)
15	10101 ¹⁸	27 ³ - 40 ⁵	68 - 100	272 - 400	2.5 (2)	4 (2)
16	10110 ¹²	25 - 46 ⁴	50 - 92	200 - 368	2 (4)	4 (2)
17	10111 ¹⁸	25 - 33 ²	100 - 132	200 - 264	4 (2)	2 (2)
18	11000 ¹²	27 ³ - 53 ⁵	68 - 132	204 - 396	2.5 (2)	3 (2)
19	11001 ¹⁸	36 ⁶ - 66 ¹	72 - 132	180 - 330	2 (2)	2.5 (2)
1A	11010 ¹²	50 ¹⁷ - 66 ¹	50 - 66	200 - 264	1 (4)	4 (2)
1B	11011 ¹⁸	33 ⁶ - 66 ¹	66 - 132	198 - 396	2 (2)	3 (2)
1C	11100 ¹²	44 ⁶ - 66 ¹	66 - 99	198 - 297	1.5 (2)	3 (2)
1D	11101 ¹²	48 ⁶ - 66 ¹	72 - 99	180 - 248	1.5 (2)	2.5(2)
1E	11110 ⁸	Not Usable			Off	Off

Table 9. MPC8245 PLL Configurations for 400-MHz Part Offering (continued)

Ref	PLL_CFG[0:4] ^{10,13}	400 MHz Part ⁹			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range ¹ (MHz)	Periph Logic/Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI to Mem (Mem VCO)	Mem to CPU (CPU VCO)
1F	11111 ⁸	Not Usable			Off	Off

- ¹ Limited by maximum PCI input frequency (66 MHz).
- ² Limited by maximum system memory interface operating frequency (133 MHz).
- ³ Limited by minimum memory VCO frequency (133 MHz).
- ⁴ Limited due to maximum memory VCO frequency (372 MHz).
- ⁵ Limited by maximum CPU operating frequency (400 MHz).
- ⁶ Limited by minimum CPU VCO frequency (360 MHz).
- ⁷ Limited by maximum CPU VCO frequency (800 MHz).
- ⁸ In clock off mode, no clocking occurs inside the MPC8245 regardless of the PCI_SYNC_IN input.
- ⁹ Range values are shown rounded down to the nearest whole number (decimal place accuracy removed) for clarity.
- ¹⁰ PLL_CFG[0:4] settings not listed (01011, 01101, 01111, 10001, 10011, 10101, 11001, and 11011) are reserved.
- ¹¹ Multiplier ratios for this PLL_CFG[0:4] setting are different from the MPC8240 and are not backwards-compatible.
- ¹² PCI_SYNC_IN range for this PLL_CFG[0:4] setting is different from the MPC8240 and may not be fully backwards-compatible.
- ¹³ Bits 7–4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value.
- ¹⁴ In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for hardware modeling support. The AC timing specifications given in this document do not apply in PLL bypass mode.
- ¹⁵ In dual PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation, and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is intended for hardware modeling support. The AC timing specifications given in this document do not apply in dual PLL bypass mode.
- ¹⁶ Limited by minimum CPU operating frequency (100 MHz).
- ¹⁷ Limited by minimum memory bus frequency (50 MHz).
- ¹⁸ PCI_SYNC_IN range for this PLL_CFG[0:4] setting does not exist on the MPC8240 and may not be fully backwards-compatible.

Table 10 compares the speeds of the MPC8240 and MPC8245.

Table 10. Maximum Speeds for MPC8240 and MPC8245

Unit	MPC8240	MPC8245
MPC603e core processor	250 MHz	400 MHz
Integrated memory controller	100 MHz SDRAM	133 MHz
AC timing specifications	—	Backward-compatible with those of the MPC8240, in consideration of T _{OS} factor. See Section 1.4.1, “General Compatibility.”

Note: The clock multipliers do not allow 133 MHz memory bus speed to be used at 300 and 350 MHz CPU speeds.

1.4 Other Compatibility Factors

This section describes general compatibility, reset configuration signal differences, and register differences between the MPC8240 and MPC8245.

1.4.1 General Compatibility

The programmable PCI output valid and output hold feature controlled by bits in power management configuration register 2, (PMCR2) <0x72>, has changed slightly in the MPC8245. For the MPC8240, three bits, PMCR2[6–4] = PCI_HOLD_DEL, are used to select one of eight possible PCI output timing configurations. PMCR2[6–5] are software-controllable, but are initially set by the reset configuration state of the machine check (\overline{MCP}) and debug clock (CKE) signals, respectively. PMCR2[4] can be changed by the software. The default configuration for PMCR2[6–4] is 0b110, since the \overline{MCP} and CKE signals have internal pull-up resistors, but this default configuration does not select 33 or 66 MHz PCI operation output timing parameters for the MPC8240; this choice is made by the software. For the MPC8245, only two bits in the power management configuration register 2 (PMCR2), PMCR2[5–4] = PCI_HOLD_DEL, control the variable PCI output timing. PMCR2[5–4] are software-controllable, but are initially set by the inverted reset configuration state of the MCP and CKE signals, respectively. The default configuration for PMCR2[5–4] is 0b00, since the \overline{MCP} and CKE signals have internal pull-up resistors and the values from these signals are inverted. This default configuration selects 66 MHz PCI operation output timing parameters. There are four programmable PCI output timing configurations on the MPC8245. For details, see the appropriate hardware specifications document.

Note that there is a timing requirement that must be considered for the MPC8245. Due to the internal delay present on the SDRAM_SYNC_IN signal with respect to the *sys_logic_clk* inputs to the DLL, the resulting SDRAM clocks become offset by the delay amount. Time delay for SDRAM_SYNC_OUT to SDRAM_SYNC_IN for the MPC8245 is out-of-phase with the SYS_LOGIC_CLK timing when the MPC8245 is used as a drop in replacement for the MPC8240. To solve this issue of timing compatibility, it is recommended that the trace length for SDRAM_SYNC_IN to SDRAM_SYNC_OUT be shortened by the timing parameter T_{os} . This parameter ranges from 0.65 to 1.0 ns. T_{os} must be implemented for new MPC8245 designs. For pre-existing MPC8240 designs using MPC8245, the delay (T_{os}) must be accounted for in the memory timing equations. The memory output valid and input setup times are improved over those of the MPC8240 and should also be taken into account when calculating memory timing backward-compatibility with the MPC8240. See Table 9 in the *MPC8245 Integrated Processor Hardware Specifications* and Application Note AN2164, *MPC8245 Memory Clock Design Guidelines*.

The MPC8245 does not support the SDRAM flow-through memory interface.

Table 11. Memory Configuration Support

Configuration Type	Memory Supported in MPC8240	Memory Supported in MPC8245
Flow-through	EDO, FPM, SDRAM	—
Registered	EDO, FPM, SDRAM	SDRAM
In-line	SDRAM	SDRAM

Note: Dynamic random access memory-type definitions: EDO—extended data out, FPM—fast page mode, SDRAM—synchronous dynamic random access memory.

Other Compatibility Factors

The MPC8240 and MPC8245 are fundamentally the same, but as with generation progressions of any product, the MPC8245 has enhancements that result in greater capabilities and frequency offerings. For more details on the MPC8240 or MPC8245, refer to the appropriate user's manual and hardware specifications documents.

1.4.2 Reset Configuration Signal Differences

Table 12 outlines the reset configuration signals which differ between the MPC8240 and MPC8245. This table represents only the reset configuration signals that differ. For more details on these and other reset configuration signals please see Section 2.4 "Configuration Signals Sampled at Reset," of the specific user's manual. Note that although the MPC8240 and MPC8245 parts use $\overline{RCS0}$ as a reset configuration signal, it is an I/O signal on the MPC8240 and an output signal on the MPC8245.

Table 12. Reset Configuration Differences

Signal	MPC8240 Meaning	MPC8245 Meaning
\overline{MCP} , CKE Default = 11	PCI output hold delay value (in ns) relative to $\overline{PCI_SYNC_IN}$. The values on these two signals determine the initial settings of $\overline{PMCR2[6-5]}$ of the power management configuration register 2—Offset 0x72.	PCI output hold delay value (in ns) relative to $\overline{PCI_SYNC_IN}$. The values on these two signals determine the initial settings of $\overline{PMCR2[5-4]}$ of the power management configuration register 2—Offset 0x72.
PMAA0 Default = 1	Driver capability for the $\overline{MDH[0:31]}$, $\overline{MDL[0:31]}$, $\overline{PAR[0:7]}$, $\overline{MAA[0:2]}$, and $\overline{RCS1}$ signals. Sets the initial value of the $\overline{DRV_MEM_CTRL[1]}$ bit in \overline{ODCR} . PMAA0 is used in combination with PMAA1, as follows: 1 20- Ω data bus drive capability; when this is selected, only 8- or 13.3- Ω drive capability allowed for PMAA1. 0 40- Ω data bus drive capability; when this is selected, only 20- or 40- Ω drive capability allowed for PMAA1.	Driver capability for some memory signals. Sets the initial value of the $\overline{DRV_MEM_CTRL[1]}$ bit in \overline{ODCR} . PMAA0 is used in combination with PMAA1, as follows: 00 reserved 01 40- Ω drive capability 10 20- Ω drive capability 11 6- Ω drive capability This bit also controls the driver capability for standard signals: $\overline{MDH[0:31]}$, $\overline{MDL[0:31]}$, $\overline{PAR[0:7]}$, $\overline{MAA[0:2]}$, \overline{SDA} , \overline{SCL} , \overline{CKO} , \overline{QACK} , $\overline{DA[10:6]}$, and \overline{MCP} . The description is as follows: 1 20- Ω drive capability 0 40- Ω drive capability
PMAA1 Default = 1	Driver capability for address signals $\overline{RAS/CS[0:7]}$, $\overline{CAS/DQM[0:7]}$, \overline{WE} , \overline{FOE} , $\overline{RCS0}$, $\overline{SDBA0}$, \overline{SDRAS} , \overline{SDCAS} , \overline{CKE} , \overline{AS} , and $\overline{SDMA[12:0]}$. Sets the initial value of the $\overline{DRV_MEM_CTRL[2]}$ bit in the \overline{ODCR} register. PMAA0 is used in combination with PMAA1, as follows: 11 8- Ω drive capability 10 13.3- Ω drive capability 01 20- Ω drive capability 00 40- Ω drive capability	Same as PMAA0, except sets the initial value of the $\overline{DRV_MEM_CTRL[2]}$ bit in \overline{ODCR} .

Table 12. Reset Configuration Differences (continued)

Signal	MPC8240 Meaning	MPC8245 Meaning
PMAA2 Default = 1 in MPC8240 Default = 1 in MPC8245	Sets the initial value of ODCR[DRV_PCI]. 0 High drive capability on PCI signals (25 Ω) 1 Medium drive capability on PCI signals (50 Ω)	Sets the initial value of ODCR[DRV_PCI]. 0 20 drive capability on AD[31:0], C/BE[3:0], DEVSEL, FRAME, GNT[4:0], PAR, INTA, IRDY, PERR, SERR, STOP, TRDY, IRQ0/S_INT, IRQ1/S_CLK, and IRQ4/L_INT signals and 6 drive capability on IRQ2/S_RST and IRQ3/S_FRAME 1 40 drive capability on PCI/EPIC signals The initial value of this bit is determined by the PMAA2 reset configuration pin.
PLL_CFG[0:4]	Must be driven at reset	Not considered as reset configuration signals, but are sampled a few clocks after the negation of HRST_CTRL and HRST_CPU.
SDMA0 Default = 1	Not considered as reset configuration signals	Controls the multiplexing between the DUART signals and the PCI_CLK[0:3] signals. 0 DUART unit signals enabled 1 PCI_CLK[0:3] used instead of the DUART unit signals
SDMA1 Default = 1	Not a reset configuration signal	0 Extended ROM addressing enabled 1 Extended ROM addressing disabled
MDH[16:31]	Not a reset configuration signal	Sets the initial value of the PCI subsystem vendor ID register (at offset 0x2C)
MDH[0:15]	Not a reset configuration signal	Sets the initial value of the PCI subsystem ID register (at offset 0x2E)

1.4.3 Register Differences

This section lists the differences of programmable registers and bits between the MPC8240 and MPC8245. For details on the functional impact of the registers, see the user's manual of the appropriate part.

1.4.3.1 Configuration Registers

Table 13 lists the differences between the MPC8240 and MPC8245 configuration registers. Note that Table 13 represents only the differences and does not include registers that are the same in the two parts.

Other Compatibility Factors

Table 13. Configuration Register Differences Between MPC8240 and MPC8245

Address Offset	Register	Bits	Bit Name	MPC8240 Description	MPC8245 Description
0x2C	Subsystem Vendor ID	15–0	None	Reserved	Value is determined at startup through configuration pins MDH[16:31] but can be programmed by software after reset.
0x2E	Subsystem ID	15–0	None	Reserved	Value is determined at startup through configuration pins MDH[0:15] but can be programmed by software after reset.
0x44	PCI General Control	5–4, 2–1	None	Reserved	Various bit functions that control retry ability of PCI read transactions, LOCK support, and latency timer disconnect.
0x70	Power Management Configuration Register 1	10	SUSP_QACK	Reserved	\overline{QACK} assertion
		6	BR1_WAKE	Reserved	$\overline{BR1}$ wake
0x72	Power Management Configuration Register 2	6–4	PCI_HOLD_DEL	The initial values of bits 6, and 5 are determined by the \overline{MCP} and CKE reset configuration signals, respectively.	The initial values of bits 5 and 4 are determined by the \overline{MCP} and CKE reset configuration signals, respectively. Bit 6 is not used in the definition of PCI_HOLD_DEL.
		1	SHARED_MCP	\overline{MCP} output signal state definition	Reserved
0x73	Output Driver Control Register	7, 5–2	Various driver-related names (DRV_xx)	Definitions based on driver capabilities specific to the MPC8240. See Table 4 of the hardware specifications for more details.	Definitions based on Driver capabilities specific to the MPC8245. See the hardware specifications and user's manual for more details.
		6	DRV_STD_MEM	Driver capability for standard signals	Reserved. See chip errata #19 for more details.
		1–0	DRV_MEM_CLK[1–2]	Controlled Driving strength of SDRAM clocks and SDRAM_SYNC_OUT	Reserved for chip Rev 1.1. Controls driving strength of SDRAM clocks and SDRAM_SYNC_OUT on chip Rev 1.2 parts.
0x74	CLK Driver Control	15	PCI_SYNC_OUT	Reserved	Disables/enables the PCI_SYNC_OUT signal.

Other Compatibility Factors

Table 13. Configuration Register Differences Between MPC8240 and MPC8245 (continued)

Address Offset	Register	Bits	Bit Name	MPC8240 Description	MPC8245 Description
0x76	Miscellaneous I/O Control Register 1	7–6, 2	Various mode-related names.	Reserved	Various bits configure the MCP and SRESET outputs, as well as the delay line length.
0x77	Miscellaneous I/O Control Register 2	5–4	SDRAM_DSCD	Reserved	Selects the minimum SDRAM_SYNC_IN input setup and hold times. See the hardware specifications document for more details.
0xA8	Processor Interface Configuration Register 1	16	ADDRESS_MAP	Controls address map used by MPC8240	Reserved
		8	DEC	Reserved	Enable/disable TBEN input of processor core in extended ROM mode
		7	NO_BUS_WIDTH_CHECK	Reserved	Controls bus width restriction of processor writes to Flash/ROM.
0xAC	Processor Interface Configuration Register 2	19–18	CF_IP1 in MPC8240 CF_SNOOP_WS in MPC8245	Internal parameter programmed based on processor-to-memory clock ratios	Snoop wait cycles. Controls the minimum number of wait states for the address phase in a snoop cycle.
		3–2	CF_IP2 in MPC8240 CF_APHASE_WS in MPC8245	Internal parameter 2	Internal address phase wait cycles
0xD0	Extended ROM Configuration Register 1	31–0	Various extended ROM bit names	Reserved	Various bits defining the data path and timing parameters for $\overline{RCS2}$
0xD4	Extended ROM Configuration Register 2	31–0	Various extended ROM bit names	Reserved	Various bits defining the data path and timing parameters for $\overline{RCS3}$
0xD8	Extended ROM Configuration Register 3	27–12	RCS2_SADDR	Reserved	Starting address for $\overline{RCS2}$ in megabytes
		3–0	RCS2_SIZE	Reserved	Encoded size of $\overline{RCS2}$
0xDC	Extended ROM Configuration Register 3	27–12	RCS3_SADDR	Reserved	Starting address for $\overline{RCS3}$ in megabytes
		3–0	RCS3_SIZE	Reserved	Encoded size of $\overline{RCS3}$

Other Compatibility Factors

Table 13. Configuration Register Differences Between MPC8240 and MPC8245 (continued)

Address Offset	Register	Bits	Bit Name	MPC8240 Description	MPC8245 Description
0xF0	Memory Control Configuration Register 1 (MCCR1)	22–21	DBUS_SIZ[0–1]	Data path width for <u>RCS0</u> , <u>RCS1</u> , (S)DRAM, and FPM/EDO systems.	Definition used in conjunction with bit 17 of MCCR4. Data path width for <u>RCS0</u> , <u>RCS1</u> , and SDRAM.
		17	RAM_TYPE (in MPC8240) SDRAM_EN (in MPC8245)	Defines RAM type	Enables SDRAM
0xF4	Memory Control Configuration Register 2 (MCCR2)	19	WRITE_PARITY_CHK in MPC8240 INLINE_WR_EN in MPC8245	Write parity check enable	In-line parity error reporting enable
		17	ECC_EN in MPC8240	ECC enable for FPM/EDO memory	Reserved
		16	EDO in MPC8240	Indicates type of DRAM for memory interface	Reserved
0xF8	Memory Control Configuration Register 3 (MCCR3)	23–20	RDLAT	Data latency from read command	Reserved (internal logic defines RDLAT)
		19–0	Various names in MPC8240	All bits are specific to DRAM/EDO timing	Reserved (since MPC8245 supports only SDRAM)
0xFC	Memory Control Configuration Register 4 (MCCR4)	21	EXTROM	Reserved	Enables Extended ROM address space
		17	DBUS_SIZE[2]	Reserved	Used along with bits 22–21 of MCCR1 to define data path width for <u>RCS0</u> , <u>RCS1</u> , and SDRAM.

1.4.3.2 Address Translation Registers

Table 14 lists the differences between the MPC8240 and MPC8245 configuration registers. Note that Table 14 represents only the differences and does not include registers that are the same in the two parts.

Table 14. Address Translation Registers ¹

Address Offset	Register(s)	Bits	Bit Name	MPC8240 Description	MPC8245 Description
	Inbound Translation Window Register ²	31	Inbound translation base address	Reserved	Local memory address—starting address for the inbound translation window
		11	No snoop enable	Reserved	In agent mode, allows snooping to be disabled on the peripheral logic bus
	Outbound Translation High Base Address Registers	31–0	—	Reserved	Defines upper 32-bit base for an outbound translation window

¹ Apart from the above, the MPC8245 has additional duplicate registers which have the same functions as their original. New duplicate registers in the MPC8245 include LMBAR1, OMBAR1, OTWR1, and ITWR1. See the user's manual for more details.

² More than one such register exists in MPC8245.

1.4.3.3 DMA Registers

Table 15 lists DMA registers that exist in the MPC8245 but not in the MPC8240. For more details, see the appropriate user's manual.

Table 15. New DMA Register Registers (Not in MPC8240)

PCI Memory Offset	Register Name on MPC8245
0x10C	DMA 0 High Current Descriptor Address Register (HCDAR)
0x114	DMA 0 High Source Address Register (HSAR)
0x11C	DMA 0 High Destination Address Register (HDAR)
0x128	DMA 0 High Next Descriptor Address Register (HNDAR)
0x20C	DMA High Current Descriptor Address Register (HCDAR)
0x214	DMA 1 High Source Address Register (HSAR)
0x21C	DMA 1 High Destination Address Register (HDAR)
0x228	DMA 1 High Next Descriptor Address Register (HNDAR)

1.4.3.4 Message Unit Registers

Table 16 lists the message unit related registers that exist in the MPC8245 but not in the MPC8240, and Table 17 lists I₂O register differences between the two devices. For more details, see the appropriate user's manual.

Table 16. New Doorbell Registers (Not in MPC8240)

PCI Memory Offset	Register Name on MPC8245
0x070	Extended Doorbell Mask Register (EDBMR)
0x078	Extended Doorbell Status Register (EDBSR)
0x080	Extended Doorbell Write 1 Clear Register (EDBW1C)
0x088	Extended Doorbell Write 1 Set Register (EDBW1S)

Table 17. I₂O Register Differences

Address Offset	Register Name	Bits	Bit Name	MPC8240 Description	MPC8245 Description
0x030	Outbound Message Interrupt Status Register (OMISR)	30, 28, 25–24, 17–16	Various	Reserved	Various doorbell, interrupt, and DMA related bit functions
0x0_0100	Inbound Message Interrupt Status Register (IMISR)	10	LWIS	Reserved	Local watchpoint interrupt status

1.4.3.5 I²C Registers

Table 18 lists the I²C related registers that exist in the MPC8245 but not in the MPC8240. For more details, see the appropriate user's manual.

Table 18. I²C Register Differences

Address Offset	Register Name	Bits	Bit Name	MPC8240 Description	MPC8245 Description
0x0_3008	I ² C Control Register (I2CCR)	1	PCII	Reserved	PCI interrupt enable
		0	BCST	Reserved	Broadcast enable
0x0_300C	I ² C Status Register (I2CSR)	3	BCA	Reserved	Broadcast address detection

1.4.3.6 EPIC Registers

Table 19 lists an EPIC register that exists in the MPC824 but not in the MPC8240. For more details, see the appropriate user's manual.

Table 19. New EPIC Registers (Not in MPC8240)

Address Offset from EUMBBAR ¹	Register Name on MPC8245
0x4_10F4	Time Control Register
0x5_1120	DUART Ch1 Interrupt Vector/priority Register (IIVPR4)
0x5_1130	DUART Ch1 Interrupt Destination Register (IIDR4)
0x5_1140	DUART Ch2 Interrupt Vector/priority Register (IIVPR5)
0x5_1150	DUART Ch2 Interrupt Destination Register (IIDR5)

¹ EUMBBAR—embedded utilities memory block base address register (address offset: 0x78).

1.4.3.7 DUART Registers

The MPC8240 does not have DUART capability, hence the DUART registers exist only in the MPC8245. The registers exist from PCI memory offset 0x500 to 0x611. See the *MPC8245 Integrated Processor User's Manual* for detailed information on these registers.

1.4.3.8 Performance Monitor Registers

The MPC8240 does not support performance monitoring, hence the performance registers exist only in the MPC8245. The registers exist from PCI memory offset 0xe00 to 0xe20. See the *MPC8245 Integrated Processor User's Manual* for detailed information on these registers.

1.4.3.9 Watchpoint Registers

Table 20 lists the watchpoint registers that exist in the MPC8245 but not in the MPC8240. For more details, see the appropriate user's manual.

Table 20. New Watchpoint Registers (Not in MPC8240)

PCI Bus Offset	Register Name in MPC8245
0xF0C	Watchpoint Data High Register (WP_DH_REG)
0xF10	Watchpoint Data Low Register (WP_DL_REG)
0xF14	Watchpoint Parity Register (WP_PAR_REG)
0xF28	Watchpoint 1 Control Monitor (WP1_CTRL_MON)
0xF2C	Watchpoint 1 Address Monitor (WP1_ADDR_MON)
0xF40	Watchpoint 2 Control Monitor (WP2_CTRL_MON)
0xF44	Watchpoint 2 Address Monitor (WP2_ADDR_MON)

1.5 Conclusion

The MPC8240 and MPC8245 have the same major functional features. The MPC8245 enhances and adds to the features of the MPC8240 and, therefore, is a more efficient part. The two parts are compatible as long as hardware and some software differences are taken into account.

1.6 Document Revision History

Table 21 details revisions and changes to this application note.

Table 21. Document Revisions

Rev. No.	Substantive Changes
0.0	Initial release, 4/3/01. Removed all references to 1.8 V \pm 100 mV part offering since Motorola will not offer it until later in the project life. The offering of 2.0 V \pm 100 mV part was kept. 5/15/01
1.0	Corrected Technology information for MPC8245 in Table 2, to 0.25 μ m. Added paragraph on timing requirement, "T _{os} " in Section 1.4. T _{os} is called T _{su} in Rev 0.3 of the hardware specifications document. This will change in future revisions of the document, with T _{os} being used consistently.
2.0	Corrected memory device information for the MPC8240 and MPC8245 in Table 1. Added 1.8 voltage information to Tables 2 and 5. Divided Section 1.4 to Sections 1.4.1 and 1.4.2, with the addition of Section 1.4.2 which covers Register Differences.
3.0	Table 2: Added information for the 333 and 350 MHz CPU parts. Noted source voltage validation for 1.8/2.0 \pm 100 mV for the 266 and 300 MHz parts. Added note to mention MPC8241 (low cost MPC8245 part). Edited footnotes and updated Table 7. Added Table 8 with PLL configurations for 333 and 350 MHz part offerings. Added a subsection to Section 1.4 to cover reset configuration signals differences (Section 1.4.2).
4.0	Replaced references to the 603e core with G2 core. Updated Figure 2 to show DMA controller and message units as being updated sections of the peripheral block. Removed shading for the central control unit block. Added note describing MPC8241 in Section 1.3. Section 1.3.1: Updated frequency listing format of first paragraph. Updated and corrected "Core Power Supply" row of Table 2. Added notes for part number number specifications of the extended temperature and the 400 MHz part offerings. Updated voltage and frequency listings of the MPC8245 in Section 1.3.1. Section 1.3.2: Updated pin type listings in Table 3, including power supply. Corrected note 6 to exclude SDMA12, since this signal was already on the MPC8240. Section 1.3.3.1: Added note on part number specifications document for temperature range information. Section 1.3.4: Corrected difference in Mem-to-CPU ratio statement which had stated that PLL configuration 0x08 was different between the MPC8240 and the MPC8245. Updated the PLL tables for the MPC8245 and added one fore the 400 MHz part offering. Section 1.4.2: Reworded format of default setting for signals in Table 11. Added information regarding driver capability for standard signals of the MPC8245 under the description for PMAA0, as per chip errata #19. Updated description information for PMAA2 in the MPC8245. Section 1.4.3.1: Table 12, added chip errata related information to 0x73 row. Removed rows regarding 0xC4 and 0xC5, since bit 6 of these registers are now functionally the same in the MPC8240 and the MPC8245, due to Errata #21 on the MPC8245. Added section on Address Translation Registers (Section 1.4.3.2). Updated description for SDMA1 and PMAA2 signals in Table 11.

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