

What are the Differences Between e500v1 and e500v2 PowerPC Cores?

- The e500v2 uses 36-bit physical addressing which is supported by the following:
 - ✓ MMU assist register 7 (MAS7)
 - ✓ HID0[EN_MAS7_UPDATE]
 - ✓ Programmable jumper options to specify the upper bits of the reset vector
- The e500v2 has 512-entry, 4-way set-associative unified TLB for TLB1
- The maximum variable page size is extended to 4Gbyte
- Embedded double-precision floating-point APU has been added. These instructions use the 64-bit GPRs as a single double-precision operands. This APU is enabled through MSR[SPE]
- Slightly different functionality of HID1[RFXE] bit
- The data line fill buffer in the LSU is expanded from three to five entries
- The load miss queue in the LSU is expanded from four to nine entries
- TBSEL and TBEE bits have been added to the performance monitor global control register 0 (PMG0) to support monitoring of time base events
- Minor modifications to the SPE APU
- Data cache flush assist capability, supported through HID0[DCFA]. When DCFA is set, the cache miss replacement algorithm ignores invalid entries and follows the replacement sequence defined by the PLRU bits. This reduces the series of uniquely addressed load or **dcbz** instructions required to flush the cache

